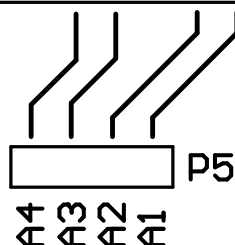
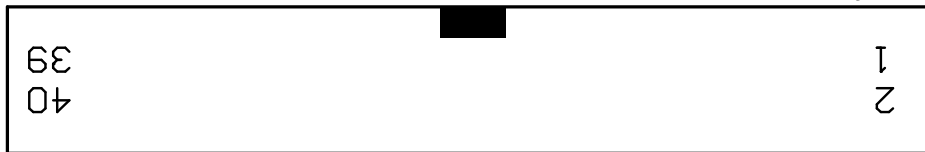
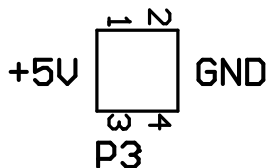
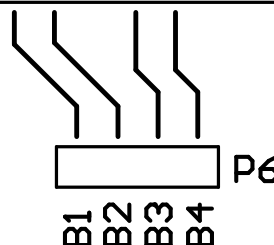


DEO FPGA CON

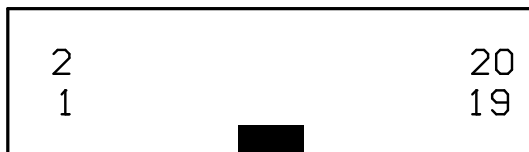


RST_N

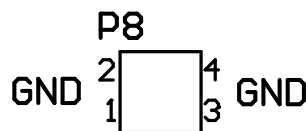


PIN MAPPING

ADAPTER	FPGA
A1	R14
A2	T12
A3	R12
A4	T10
B1	T15
B2	W17
B3	AB17
B4	AA18
RST_N	AA9



XK-1 Node 0



P7

RST_N
TDOC
DEBUG
TCK
TMS
TDI
TRST_N



XK-1 Node 1

NO	PIN	DIR	N1	PIN	WIRE MAP
A1		← 1	B1		
A2		← 0	B2		
A3		→ 0	B3		
A4		→ 1	B4		

Dual XK-1 Adapter Board
For XMOS LINK to FPGA
By Bianco Zandbergen